AMENDMENTS TO THE DRAWINGS

Applicant submits herewith one replacement sheet for FIG. 4, which has been amended to more clearly show the connection of the computer readable medium 400 to a computer 410 and to a receiver device 420, consistent with an exemplary embodiment of the present invention.

Applicant respectfully requests that the Examiner approve the replacement drawing sheet (FIG. 4).

Attachment: One replacement Sheet (FIG. 4)

REMARKS

I. Status of Application

Claims 1 and 3-8 are all the claims pending in the application. Claims 1 and 3-8 presently stand rejected.

II. Objections to the Drawings

The Examiner has objected to the drawings alleging that the claimed "a computer readable medium" and its connection with the present invention apparatus must be shown or the features canceled from the claims. Without conceding to the merits of the Examiner's objections, Applicant has submitted herewith a replacement sheet for FIG. 4, which has been amended to more clearly show the connection of the computer readable medium 400 to a computer 410 and to a receiver device 420, consistent with an exemplary embodiment of the present invention. No new matter has been added.

Accordingly, Applicant respectfully requests that the Examiner withdraw these objections.

III. Claim Rejections Under 35 U.S.C. § 112

Claim 8 is rejected under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the enablement requirement. Specifically, the grounds of rejection allege that:

> "Claim 8 claimed 'a computer readable medium encoded with a computer program for generating a clock signal out of an electrical data signal'. However, the specification and drawing do not provide any specific detail to teach 'a computer readable medium encoded with a computer program for generating a clock signal out of an electrical data signal' and how a computer readable medium encoded with a computer program generates a clock signal, specially the connection between the computer readable medium and the present invention apparatus. Without

> such detail description, the disclosure does not enable a person of ordinary to made and use the claimed invention."

Applicant respectfully disagrees with the grounds of rejection. As an initial matter, claim 8 does not recite "a computer readable medium encoded with a computer program for generating a clock signal out of an electrical data signal," as alleged by the grounds of rejection. To the contrary, claim 8 plainly recites (among other things), "[a] computer-readable medium encoded with a computer program which causes a computer to generate a clock signal out of an electrical data signal that is received by a receiver" (emphasis added). Thus, the grounds of rejection are improper *at least* because they inaccurately address the recitations of claim 8.

Further, since claim 8 does not recite "a computer readable medium encoded with a computer program for generating a clock signal out of an electrical data signal," as alleged by the grounds of rejection, the Examiner's allegation that the specification must teach "how a computer readable medium encoded with a computer program generates a clock signal, specially the connection between the computer readable medium and the present invention apparatus" is unsupported and irrelevant.

Finally, Applicant submits that the recitations in claim 8 of "a computer-readable medium encoded with a computer program which causes a computer to generate a clock signal out of an electrical data signal that is received by a receiver," clearly satisfy the enablement requirement. The test of enablement is whether one reasonably skilled in the art could make or use the invention from the disclosures in the patent coupled with information known in the art

without undue experimentation.[1] MPEP § 2164.01(a) specifies that there are many factors to be considered when determining whether a disclosure satisfies the enablement requirement and whether any necessary experimentation is "undue." The factors include, but are not limited to:

(A) The breadth of the claims;

(B) The nature of the invention;

(C) The state of the prior art;

(D) The level of one of ordinary skill;

(E) The level of predictability in the art;

(F) The amount of direction provided by the inventor;

(G) The existence of working examples; and

(H) The quantity of experimentation needed to make or use the invention.

Here, the grounds of rejection do not address any of the above factors. It is improper to conclude that a disclosure is not enabling while ignoring the above factors. The Examiner's analysis must consider all the evidence related to each of these factors, and any conclusion of non-enablement must be based on the evidence as a whole. *See* MPEP § 2164.01(a).

Moreover, Applicant submits that one reasonably skilled in the art could make or use a computer-readable medium encoded with a computer program which causes a computer to generate a clock signal out of an electrical data signal, as recited in claim 8, from *at least* claim 8 and paragraph 0018 of the original specification, coupled with information known in the art,

[1] *United States v. Telectronics, Inc.*, 857 F.2d 778, 785, 8 USPQ2d 1217, 1223 (Fed. Cir. 1988). See also: *Mineral Separation v. Hyde*, 242 U.S. 261, 270 (1916); *In re Wands*, 858 F.2d 731, 737, 8 USPQ2d 1400, 1404 (Fed. Cir. 1988); and MPEP § 2164.01.

without undue experimentation. Accordingly, Applicant respectfully requests that the Examiner withdraw this rejection for *at least* the aforementioned reasons.

Nevertheless, without conceding the merits of the Examiner's rejections, Applicant has amended the specification and drawings, as set forth herein, to more clearly describe the connection between the computer 410 and the receiver device 420. Therefore, Applicant submits that claim 8 satisfies the enablement requirement for *at least* these additional reasons.

IV. Claim Rejections Under 35 U.S.C. § 103

Claims 1 and 3-8 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Pathak et al. (7,158,727) in view of newly cited LaGasse et al. (2003/0020985). Applicant respectfully traverses all of these rejections for *at least* the reasons set forth below.

First, independent claim 1 plainly recites (among other things):

> ...wherein the frequency-multiplied signal is used to drive the phase locked loop circuit...

The grounds of rejection fail to point to any aspect of the cited references that teaches or suggests these features. The grounds of rejection also fail to even allege that it would have been obvious to achieve the above recitations in view of Pathak and LaGasse. In fact, the grounds of rejection ignore the above recitations altogether.

Further, even if one were to replace Pathak's clock recovery unit 103 with LaGasse's clock recovery unit 150 comprising a phased locked loop 154, as alleged by the grounds of rejection, one still would not arrive at the claimed invention. Indeed, such a modification of Pathak's teachings with LaGasse would still fail to teach or suggest the claimed features of wherein the frequency-multiplied signal is used to drive the phase locked loop circuit, as recited

in claim 1. Neither Pathak, LaGasse, nor any combination thereof, provides any teaching or suggestion whatsoever to replace Pathak's clock recovery unit 103 with LaGasse's clock recovery unit 150, and to thereafter modify such a combination so that a frequency-multiplied signal produced by Pathak's electrical to optical converter / 4:1 multiplexer 108 is used to drive the phase locked loop 154. Moreover, the grounds of rejection have failed to identify any such teaching or suggestion. Thus, claim 1 is patentable over the cited references for *at least* these reasons.

Second, independent claim 1 further recites:

> ...a frequency multiplicator unit, which frequency-multiplies the converted electrical data signal, thereby producing a frequency-multiplied signal...

The grounds of rejection allege that Pathak's electrical-to-optical converter / 4:1 multiplexer 108 corresponds to a frequency multiplicator unit, as claimed. Applicant respectfully disagrees with the grounds of rejection.

As previously explained with the Amendment filed on December 10, 2007, Pathak bears no relevance at all to the invention recited in claim 1 since Pathak does not relate in any way to the question of how a clock signal is recovered from a distorted optical signal. As further explained in the Amendment filed on December 10, 2007, the feature of frequency multiplication is substantially different from the feature of demultiplexing as disclosed in Pathak. Accordingly, the Examiner's interpretation of a frequency multiplicator unit, which frequency-multiplies the converted electrical data signal, as including a demultiplexer, like that disclosed in Pathak, is not reasonable, as required by the MPEP §2111.01.

Indeed, a skilled artisan would recognize that frequency multiplication refers to an analog technique used to achieve a spectral transformation. In contrast, a skilled artisan would recognize that demultiplexing is a completely different process of deinterleaving bit streams, which are necessarily digital (not analog).

The grounds of rejection have failed to provide any evidence in fact and/or reasoning to rebut Applicant's previous arguments to this effect and, thus, claim 1 is patentable for *at least* the reasons already of record. In addition, MPEP §707.07(f) requires that "[w]here the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, take note of the applicant's argument and answer the substance of it" (emphasis added). The grounds of rejection do not satisfy the requirements of MPEP §707.07(f) since they do not even attempt to answer the substance of Applicant's previous arguments.

Third, without conceding to the merits of the Examiner's rejections, Applicant has amended claim 1, as set forth above, to recite (among other things):

> ...wherein said frequency multiplication is an analog signal processing technique.

These amendments are supported by *at least* FIG. 1 of the original specification, which shows an analog spectrum wherein the signal is filtered after O/E conversion (i.e. prior to sampling/AD conversion). Hence, it is clear from FIG. 1, and the corresponding description thereof, that the signal processing is analog.

As already discussed, the feature of frequency multiplication, which is an analog signal processing technique, is completely different from Pathak's feature of demultiplexing, which is a process of deinterleaving bit streams, which are necessarily digital (not analog).

Therefore, claim 1 is patentable over the cited references for *at least* these reasons. Moreover, the dependent claims 3-7 are allowable *at least* by virtue of their dependency. Thus, Applicant respectfully requests that the Examiner withdraw these rejections.

B. Independent Claim 8

In view of the similarity between the requirements of claim 8 and the requirements discussed above with respect to independent claim 1, Applicant respectfully submits that arguments analogous to the foregoing arguments as to the patentability of independent claim 1 demonstrate the patentability of claim 8. As such, it is respectfully submitted that claim 8 is patentably distinguishable over the cited references *at least* for reasons analogous to those presented above. Thus, the allowance of this claim is respectfully solicited of the Examiner.

V. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

/ Andrew J. Taska /

Andrew J. Taska
Registration No. 54,666

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE
23373
CUSTOMER NUMBER

Date: December 22, 2008